Amendments to the Claims

Claims 1-25 (Canceled).

26. (Currently Amended): Memory circuitry comprising:

a semiconductor substrate;

a plurality of word lines received over the semiconductor substrate;

an insulative layer received over the word lines and the substrate, the insulative layer comprising at least a single well formed therein, the well comprising a base received over the word lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within said single well over the word lines;

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array; and

the insulative layer has a substantially planar outermost surface, and the capacitors ~~have capacitor~~ have inner capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

27. (Original): The memory circuitry of claim 26 wherein the base is substantially planar.

28. (Original): The memory circuitry of claim 26 wherein the word lines have insulative caps and the well base has a lowest portion which is received at least 2000 Angstroms above the caps.

29. (Original): The memory circuitry of claim 26 comprising buried digit lines, the well base having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

30. (Original): The memory circuitry of claim 26 comprising buried digit lines and wherein the base is substantially planar, and the well base being received at least 1000 Angstroms above outermost tops of the digit lines.

Claim 31 (Canceled).

32. (Currently Amended): The memory circuitry of claim 26 wherein ~~the capacitor~~ the inner capacitor storage node electrodes have topmost surfaces which are received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

Claims 33-53 (Canceled).

54. (Currently Amended): The memory circuitry of claim 26 wherein ~~individual of the capacitors have a storage node electrode,~~ at least one of ~~the storage~~ the inner storage node electrodes ~~being spaced~~ is spaced laterally inward of the outline peripherally defined by the well thereby forming a space between said one electrode and said outline.

Claims 55-57 (Canceled).

58. (Previously Presented): The memory circuitry of claim 26 wherein the memory cell storage capacitors respectively comprise an outer cell electrode having a topmost surface which is received elevationally outward of the insulative layer.

Claim 59 (Canceled).

60. (New): The memory circuitry of claim 26 wherein the inner capacitor storage node electrodes respectively comprise a portion having a container shape.

61. (New): The memory circuitry of claim 60 comprising openings formed in the well base within which individual of the inner capacitor storage nodes are received, only part of the respective portions being received within the respective openings.